WHAT IS CLAIMED IS:

1. A method of designing a semiconductor interconnect architecture including a pair of metal layers interconnected by a plurality of conductive vias, the method comprising:

identifying a via-to-metal area ratio value below which stress on a via does not significantly increase relative to stress on the via above the value; and

requiring the semiconductor interconnect architecture to have a via-to-metal area ratio at least as large as said value.

2. The method of Claim 1, wherein said value is approximately 1/100.

3. The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

4. The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

5. The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.

6. A method of producing a semiconductor interconnect architecture, the method comprising:

providing a first metal layer;

providing a second metal layer; and

providing a plurality of conductive vias interconnecting said first and second metal layers and achieving a via-to-metal area ratio at least as large as a predetermined via-to-metal area ratio value below which stress on the vias does not significantly increase relative to stress on the vias above the value.

7. The method of Claim 6, wherein said value is approximately 1/100.

8. The method of Claim 7, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

9. The method of Claim 7, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

10. The method of Claim 7, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.

11. A semiconductor interconnect architecture, the architecture comprising:

a first metal layer;

a second metal layer; and

a plurality of conductive vias interconnecting said first and second metal layers, said vias and said metal layers cooperable to provide a via-to-metal area ratio at least as large as a predetermined via-to-metal area ratio value below which stress on the vias does not significantly increase relative to stress on the vias above the value.

12. The semiconductor interconnect architecture of Claim 11, wherein said value is approximately 1/100.

13. The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

14. The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

15. The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.